UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,823	06/01/2004	Che-Hui Chang Chien	13353-US-PA	3822

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
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EXAMINER
NGUYEN, TANH Q

ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
11/16/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

	Application No.	Applicant(s)
Office Action Summary	10/709,823	CHANG CHIEN ET AL.
	Examiner	Art Unit
	Tanh Q. Nguyen	2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>21 August 2007</u>.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-9</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1-9</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on <u>01 June 2004</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

    1.☐ Certified copies of the priority documents have been received.

    2.☐ Certified copies of the priority documents have been received in Application No. _____.

    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Specification

1.   If applicant wishes to have the title printed on the patent without the brackets, the

brackets in the title needs to be removed to read:

INTERFACE AND SYSTEM FOR TRANSMITTING REAL-TIME DATA

The examiner notes that applicant indicates that the brackets in the title are

inserted automatically by the ESF system. The examiner, however, believes that the

title would be printed with the brackets without further action from applicant - see US

2005/0268019 A1 for evidence.

Claim Objections

2.   Claims 1, 3, 5, 8, 9 are objected to because of the following informalities:

"suitable for transmitting" in line 3 of claim 1 should be replaced with --the real-

time data transmission interface being suitable for transmitting-- for clarity

"when the flag indicating the state of the 3-state buffer in the flag register is

setting/reading, the 3-state buffer is in an "on" state, when the flag indicating the state of

the 3-state buffer is not setting/reading, and the 3-state buffer is in a high impedance

state" in lines 2-5 of claim 3 should be replaced with --wherein when the flag in the flag

register is setting/reading, the 3-state buffer is in an "on" state, and wherein when the

flag indicating the state of the 3-state buffer is not setting/reading, the 3-state buffer is in

a high impedance state-- for clarity

"a read/write operation" in line 3 of claim 5 should be replaced with --an

input/output operation-- to be consistent with the remaining limitations pertaining to

operations of the I/O unit

"to convert a type of the real-time data from TTL to differential or in reverse" in

lines 4-5 of claim 8 should be replaced with --to convert the real-time data from TTL to

differential, or from differential to TTL-- for clarity

"for running a microcode instruction and" in lines 5-6 of claim 9 should be deleted

because a sequencer does not run a microcode instruction and because the claim

recites "a processor...for running the microcode instruction" in lines 11-12.

Claim Rejections - 35 USC § 112

3.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of
> making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the
> art to which it pertains, or with which it is most nearly connected, to make and use the same and shall
> set forth the best mode contemplated by the inventor of carrying out his invention.

4.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter, which the applicant regards as his invention.

5.   Claims 2-4 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply

with the enablement requirement. The claim(s) contains subject matter, which was not

described in the specification in such a way as to enable one skilled in the art to which it

pertains, or with which it is most nearly connected, to make and/or use the invention.

The examiner cannot find support for "a control signal latch coupled to the bus interface

unit via the internal data bus, wherein **the data output latch** is a latch **for latching a**

control signal transmitted from the nonreal-time data interface unit to the other units",

as recited in lines 11-13 of claim 2. <u>The examiner notes that section [0027] cited by</u>

<u>applicant does not support a **data output** latch [303, FIG. 3] latching a **control** signal.</u>

6.   Claim 5 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with

the enablement requirement. The claim(s) contains subject matter, which was not

described in the specification in such a way as to enable one skilled in the art to which it

pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 5 recites "the control logic unit controls the data output latch to latch the nonreal-

time data, and determines whether to output the nonreal-time data from the data output

latch" in lines 9-11. The limitation "the control logic unit controls the data output latch to

latch the nonreal-time data" implies that the nonreal-time data **is outputted** form the

data output latch, and the limitation "the control logic...determines whether to output the

nonreal-time data" implies that the nonreal-time data **may not be outputted** from the

data output latch. One of skilled in the art would not know how to practice the invention

with the control unit determining not to output the nonreal-time data, but at the same

time controlling the data output latch to latch the nonreal-time data. <u>One of skilled in the</u>

<u>art would instead understand that the control logic unit determines whether to output</u>

<u>nonreal-time data, and to latch the nonreal-time data to the data output latch when the</u>

<u>control logic unit determines to output the nonreal-time data.</u>

7.   Claim 9 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with

the enablement requirement. The claim(s) contains subject matter, which was not

described in the specification in such a way as to enable one skilled in the art to which it

pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 9 recites "the sequencer for caching the external condition" in line 7. One skilled in the art would expect a device to cache data, <u>or data representing a condition</u>, but would not expect the device to cache a condition.

8.   Claims 2-5, 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites an "internal data bus" in line 5 - which suggests a bus for transferring data. Claim 2 also recites "a control signal latch coupled to the bus interface unit via the internal data bus" - which suggests that an internal control bus instead. <u>The examiner suggests that applicant replace "internal data bus" with --internal bus-- in the claims, and also in the specification (drawings and text) for clarity</u>.

Claim 5 recites "the data output from the I/O unit" in lines 6-7. There is insufficient antecedent basis for the limitation in the claim.

Claim 5 recites "the control logic unit controls the data output latch to latch the nonreal-time data, and determines whether to output the nonreal-time data from the data output latch" in lines 9-11. The limitation is ambiguous because "the control logic unit controls the data output latch to latch the nonreal-time data" implies that the nonreal-time data is outputted from the data output latch, and because "the control logic...determines whether to output the nonreal-time data from the data output latch" implies that the nonreal-time data may not be outputted from the data output latch. Clarification is required <u>because it is not clear why or how the nonreal-time data is latched to the data output latch and not being outputted from the data output latch</u>.

Claim 9 recites "the sequencer for caching the external condition, which is used

by the sequencer for its determining" in lines 7-8. It is not clear how the sequencer can

cache a condition, as a condition is not cacheable (only data is cacheable). In addition,

there is insufficient antecedent basis for "its determining".

9.   The rejections that follow are based on the examiner's best interpretation of the

claims.

Claim Rejections - 35 USC § 103

10.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

11.   Claims 1, 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Sparr et al. (US 2002/0176390 A1).

12.   <u>As per claim 1</u>, Sparr teaches a real-time data transmission interface [246, 235 -

FIG. 4] coupled between a real-time system for providing real-time data [[0063], lines 5-

7] and a host computer [245, FIG. 4] for providing nonreal-time data [[0063], line 1], the

real-time data transmission interface being suitable for transmitting the nonreal-time

data [290, FIG. 5] in real-time from the host computer to the real-time system [294, FIG.

5], and for transmitting the real-time data [293, FIG. 5] in nonreal-time from the real-time

system to the host computer [289, FIG. 5], the real-time data transmission interface

comprising:

a nonreal-time data interface unit [251, 258 - FIG. 5] for receiving/transmitting the

nonreal-time data;

an I/O unit [connections and ports from bus interface 251 to FIFO 295, FIG. 5]

coupled to the nonreal-time data interface unit and being used as a transmission

interface for the nonreal-time data and the real-time data [used as transmission

interface for nonreal-time data 290 and real-time data 289, FIG. 5];

a memory unit [295, FIG. 5] coupled to the I/O unit for caching the nonreal-time

data [292, FIG. 5] and the real-time data [291, FIG. 5]; and

a network interface control unit [293, 294 - FIG. 5; 235, 273 - FIG. 4] coupled to

the memory unit for receiving/transmitting the real-time data.

Sparr therefore teaches the invention except for the real-time system being a

radar system.

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to use the real-time data transmission interface of Sparr with a

radar system being a real-time system because a radar system is no more than a

system of a set of real-time systems, and because the use of a radar system with the

real-time data transmission interface of Sparr would yield the predictable results of the

real-time data transmission interface being suitable for transmitting nonreal-time data

from the host computer to the radar system and transmitting the real-time data in

nonreal-time from the radar system to the host computer. *See KSR International Co. v.*

Teleflex Inc., 82 USPQ2d 1385 (2007).

It would have been also obvious to one of ordinary skill in the art at the time the invention was made to use the real-time data transmission interface of Sparr with a radar system instead of the real-time system of Sparr because the substitution of a the real-time system of Sparr with a radar system would yield the predictable results of the real-time data transmission interface being suitable for transmitting nonreal-time data from the host computer to the radar system and transmitting the real-time data in nonreal-time from the radar system to the host computer. *See KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (2007).*

It would have been also obvious to one of ordinary skill in the art at the time the invention was made to use the real-time data transmission interface of Sparr with a radar system instead of the real-time system of Sparr because the substitution of a the real-time system of Sparr with a radar system are within the ordinary capabilities of one of ordinary skill in the art. *See KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (2007).*

Furthermore, since the real-time system of Sparr is a system of a set of real-time systems and since a radar system is another system of the set of real-time systems, the radar system is therefore no more than an obvious variant of the real-time system of Sparr. It would have been also obvious to one of ordinary skill in the art at the time the invention was made to use the real-time data transmission interface of Sparr with a radar system instead of the real-time system of Sparr because the radar system in no more than an obvious variant of the real-time system of Sparr.

Furthermore, since applicant discloses a radar system being an example of a

real-time signal processing apparatus [page 2, [0005], lines 5-6], and since applicant

does not indicate the radar system being critical to the invention, it would have been

obvious to one of ordinary skill in the art at the time the invention was made that the use

of a radar system in applicant's disclosure is application specific. Patentability cannot

be accorded to an invention merely because it is directed to a specific application

13.   As per claims 6-7, Sparr teaches the memory unit comprising:

a control logic unit [253, FIG. 5] for controlling the memory unit according to an

external control signal [[0068], lines 1-4];

a first address counter [254, FIG. 5; [0068], lines 4-6; [0067], lines 6-10] coupled

to the control logic unit for providing a first address;

a first memory [292, FIG. 5] coupled to the first address counter for storing the

nonreal-time data;

a first buffer latch unit (a latch unit is necessary to move nonreal-time data into

the first memory) coupled to the first memory via an internal bus [281, 290, 289 - FIG. 5]

for working as an input/output interface of the first memory [[0066], line 3; [0068], lines

4-6];

a second address counter [254, FIG. 5; [0068], lines 4-6; [0067], lines 6-10]

coupled to the control logic unit for providing a second address;

a second memory [291, FIG. 5] coupled to the second address counter for

storing the real-time data; and

a second buffer latch unit (a latch unit is necessary to move real-time data out of

the second memory) coupled to the second memory via the internal data bus [281, 289,

290 - FIG. 5] for working as an input/output interface of the second memory [[0066], line 3; [0068], lines 4-6].

Sparr further teaches the memory unit comprising a flag register [254, 255 - FIG. 5] for storing a flag indicating a state of the memory unit [[0068], lines 4-6; [0089], lines 6-7].

14.   Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sparr et al. in view of Christopher et al. (US 5,220,211).

Sparr teaches a programmable interface controller [222, FIG. 5], but does not teach the network interface control unit comprising a TTL/differential level converting interface, wherein the TTL/differential level converting interface is used to convert real-time data from TTL to differential or from differential to TTL.

Christopher teaches using a TTL/differential level converting interface [CV1, CV2 - FIG. 2] to convert data from TTL to differential, from differential to TTL - in order to minimize noise radiation [col. 6, lines 14-22; col. 6, lines 27-31; col. 6, lines 48-55]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a TTL/differential level converting interface, as is taught by Christopher, in order to minimize noise radiation.

Examiner's note: *Examiner has cited particular page, column and line number(s) in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. Applicant needs to consider the references in their entirety as potentially teaching*

all or part of the claimed invention.

*In the case of amending the claimed invention, Applicant is respectfully
requested to indicate the portion(s) of the specification which dictate(s) the structure
relied on for proper interpretation and verification of the metes and bounds
of the claimed invention.*

Response to Arguments

15.   Applicant's arguments with respect to the pending claims have been considered

but are moot in view of the new ground(s) of rejection.

Note that some of the 112 rejections made in the previous office action are

repeated in this office action with additional explanations and/or suggestions in the 112

rejections above to clarify the examiner position in the previous action, and to help

applicant understand the 112 rejections made in the previous office action (see

underlined portions).

In addition, if applicant traverses an obviousness rejection under 35 USC 103, a

reasoned statement must be included explaining why applicant believes the Office has

erred substantively as to the factual findings or the conclusion of obviousness. 37 CFR

1.111(b)

Conclusion

16.   Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

17.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tanh Q. Nguyen whose telephone number is 571-272-

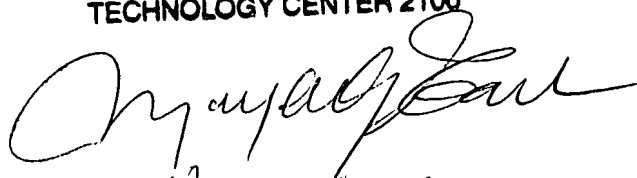4154. The examiner can normally be reached on M-F 9:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Alford Kindred can be reached on 571-272-4037. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

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system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TANH Q NGUYEN
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100

November 6, 2007